IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

HOON KIM

Serial No.:	10/798,574	Examiner:	FLYNN, NATHAN J.
Filed:	12 March 2004	Art Unit:	2826

For: THIN FILM TRANSISTOR AND METHOD FOR FABRICATING THE SAME

INFORMATION DISCLOSURE STATEMENT

Mail Stop: OFFICE OF SPECIAL PROGRAMS
Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §1.56, and §§1.97 and 1.98 as amended, Applicant cites, describes, and provides copies of the following art references:

U.S. PATENT REFERENCES:

- U.S. Patent No. 6,777,747 to Yedinak *et al.*, entitled *THICK BUFFER REGION DESIGN TO IMPROVE IGBT SELF-CLAMPED INDUCTIVE SWITCHING (SCIS) ENERGY DENSITY AND DEVICE MANUFACTURABILITY,* issued on 17 August 2004;

- U.S. Patent No. 6,534,788 to Yeo *et al.*, entitled *THIN FILM TRANSISTOR HAVING DUAL GATE STRUCTURE AND A FABRICATING METHOD THEREOF*, issued on 18 March 2003;

- U.S. Patent No. 6,528,855 to Ye *et al.*, entitled *MOSFET HAVING A LOW ASPECT RATIO BETWEEN THE GATE AND THE SOURCE/DRAIN*, issued on 4 March 2003;

- U.S. Patent No. 6,509,234 to Krivokapic, entitled *METHOD OF FABRICATING AN ULTRA-THIN FULLY DEPLETED SOI DEVICE WITH T-SHAPED GATE,* issued on 21 January 2003;

- U.S. Patent No. 6,396,079 to Hayashi *et al.*, entitled *THIN FILM SEMICONDUCTOR DEVICE HAVING A BUFFER LAYER,* issued on 28 May 2002;

- U.S. Patent No. 6,033,941 to Yang, entitled *METHOD OF FORMING A THIN FILM TRANSISTOR WITH ASYMMETRICALLY ARRANGED GATE ELECTRODE AND OFFSET REGION,* issued on 7 March 2000;

- U.S. Patent No. 5,510,640 to Shindo, entitled *SEMICONDUCTOR DEVICE AND PROCESS FOR PREPARING THE SAME,*issued on 23 April 1996;

- U.S. Patent No. 5,196,717 to Hiroki *et al.*, entitled *FIELD EFFECT TRANSISTOR TYPE PHOTO-DETECTOR,* issued on 23 March 1993;

- U.S. Patent No. 5,173,753 to Wu, entitled *INVERTED COPLANAR AMORPHOUS SILICON THIN FILM TRANSISTOR WHICH PROVIDES SMALL CONTACT CAPACITANCE AND RESISTANCE,* issued on 22 December 1992;

- U.S. Patent No. 5,144,401 to Ogura *et al.*, entitled *TURN-ON/OFF DRIVING TECHNIQUE FOR INSULATED GATE THYRISTOR,* issued on 1 September 1992;

- U.S. Patent No. 4,715,930 to Diem, entitled *PROCESS FOR PRODUCING BY SLOPING ETCHING A THIN FILM TRANSISTOR WITH A SELF-ALIGNED GATE WITH RESPECT TO THE DRAIN AND SOURCE THEREOF,* issued on 29 December 1987;

- U.S. Patent No. 4,287,661 to Stoffel, entitled *METHOD FOR MAKING AN IMPROVED POLYSILICON CONDUCTOR STRUCTURE UTILIZING REACTIVE-ION ETCHING AND THERMAL OXIDATION,* issued 8 September 1981;

- U.S. Patent No. 4,035,198 to Dennard *et al.*, entitled *METHOD OF FABRICATING FIELD EFFECT TRANSISTORS HAVING SELF-REGISTERING ELECTRICAL CONNECTIONS BETWEEN GATE ELECTRODES AND METALLIC INTERCONNECTION LINES, AND FABRICATION OF INTEGRATED CIRCUITS CONTAINING THE TRANSISTORS,* issued 12 July 1977;

- U.S. Publication No. 2004-0173812 to Currie *et al.*, entitled *SHALLOW TRENCH ISOLATION PROCESS*, published 9 September 2004;

- U.S. Publication No. 2004-0084722 to Yamaguchi *et al.*, entitled *POWER SEMICONDUCTOR DEVICE*, published 6 May 2004;

- U.S Publication No. 2004-0005740 to Lochtefeld *et al.*, entitled *STRAINED-SEMICONDUCTOR-ON-INSULATOR DEVICE STRUCTURES*, published 8 January 2004;

- U.S. Publication No. 2003-0122178 to Yang, entitled *METHOD FOR FABRICATING A FLASH MEMORY HAVING A T-SHAPED FLOATING GATE*, published 3 July 2003;

- U.S. Publication No. 2002-0054247 to Hwang *et al.*, entitled *METHOD FOR FABRICATING AN ARRAY SUBSTRATE OF A LIQUID CRYSTAL DISPLAY DEVICE*, published 9 May 2002; and

- U.S. Patent No. 6,746,904 to Van der Zaag *et al.*, entitled *ELECTRONIC DEVICES COMPRISING THIN FILM TRANSISTORS*, published on 8 June 2004.

FOREIGN PATENT REFERENCES:

- Japanese Patent Publication No. 63-093150 to Minami *et al.*, entitled *SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF*, published on 23 April 1988;

- Japanese Patent Publication No. 61-078138 to Anraku *et al.*, entitled *MANUFACTURE OF SEMICONDUCTOR DEVICE*, published on 21 April 1986;

- Japanese Patent Publication No. 02-031464 to Kawarasaki *et al.*, entitled *SEMICONDUCTOR DEVICE*, 1 February 1990;

- Japanese Patent Publication No. 2004-153112 to Yamaguchi *et al.*, entitled *POWER SEMICONDUCTOR DEVICE*, published on 27 May 2004;

- Japanese Patent Publication No. 04-096337 to Kawasaki, entitled *MANUFACTURE OF SEMICONDUCTOR DEVICE*, published on 27 March 1992;

- Japanese Patent Publication No. 04-101432 to Akiyama, entitled *MANUFACTURE*

OF MIS-TYPE TRANSISTOR, published on 2 April 1992;

- Japanese Patent Publication No. 02-281634 to Yamamoto, entitled *MANUFACTURE OF VERTICAL FIELD EFFECT TRANSISTOR*, published on 19 November 1990;

- Japanese Patent Publication No. 2002-329860 to Lee, entitled *HIGH VOLTAGE ELEMENT AND ITS MANUFACTURING METHOD*, published on 15 November 2002;

- Japanese Patent Publication No. 01-128575 to Kawamura, entitled *MANUFACTURE OF SEMICONDUCTOR DEVICE*, published on 22 May 1989;

- Korean Patent Publication No. 010082828 to Kwon, entitled *LIQUID CRYSTAL DISPLAY AND METHOD FOR MANUFACTURING THE SAME*, published on 31 August 2001;

- Korean Patent Publication No. 100332124 to Eom, entitled *METHOD FOR FORMING GATE ELECTRODE IN SEMICONDUCTOR DEVICE*, published on 28 March 2002; and

- Japanese Patent Publication No. 2001-125135 to Kawachi *et al.*, entitled *LIQUID CRYSTAL DISPLAY AND METHOD FOR MANUFACTURING THE SAME*, published on 11 May 2001.

DISCUSSION

Yedinak *et al.* '747 discloses that an IGBT has a thick buffer region with increased doping to improve self-clamped inductive switching and device manufacture. A planar or trench gate IGBT

has a buffer layer more than 25 microns thick. The buffer layer is doped high enough so that its carriers are more numerous than minority carriers, particularly at the transition between the N buffer & N drift region.

Yeo *et al.* '788 relates to a thin film transistor and a fabricating method thereof, wherein the source and drain wires are located on a substrate and a double gate structure is provided, whereby the driving capacity of on-current is improved and the degradation of a device is reduced. The TFT includes a substrate, a source electrode, a drain electrode and a lower gate electrode on the substrate, a buffer layer covering an exposed surface of the substrate as well as the source, drain and lower gate electrodes. An active layer is formed on the buffer layer, wherein a source region, a drain region, lightly-doped (LD) regions and a channel region are formed in the active layer. A gate insulating layer is formed on the channel and LD regions. An upper gate electrode is then formed on the gate insulating layer over the channel region. A passivation layer then covers the upper gate electrode. A plurality of contact holes are formed in the buffer and passivation layers, wherein the contact holes expose the source and drain electrodes and the source and drain regions. A first interconnection wire connects the source electrode to the source region. A second interconnection wire connects the drain electrode to the drain region.

Ye *et al.* '855 discloses that a MOSFET having a new source/drain (S/D) structure is particularly adapted to smaller feature sizes of modern CMOS technology. The S/D conductors are located on the shallow trench isolation (STI) to achieve low junction leakage and low junction capacitance. The S/D junction depth is defined by an STI etch step (according to a first method of making the MOSFET) or a silicon etch step (according to a second method of making the MOSFET). By controlling the etch depth, a very shallow junction depth is achieved. There is a low variation of gate length, since the gate area is defined by etching crystal silicon, not by etching polycrystalline silicon. There is a low aspect ratio between the gate and the S/D, since the gate conductor and the source and drain conductors are aligned on same level. A suicide technique is applied to the source and drain for low parasitic resistance; however, this will not result in severe S/D junction leakage,

since the source and drain conductors sit on the STI.

Krivokapic '234 discloses that a method of forming a fully depleted semiconductor-on-insulator (SOI) field effect transistor (FET). The method includes forming a T-shaped gate electrode formed at least in part in a recess formed in a layer of semiconductor material and over a body region that is disposed between a source and a drain. The method includes spacing the gate electrode from the body by a gate dielectric made from a high-K material.

Hayashi *et al.* '079 discloses that a thin film semiconductor device having improved operating characteristics and reliability of a thin film transistor formed on a glass substrate. The thin film semiconductor device has a thin film transistor 3 formed on a glass substrate 1 containing alkali metal. The surface of the glass substrate 1 is covered by a buffer layer 2. The thin film transistor 3 formed on this buffer layer 2 has a polycrystalline semiconductor thin film 4 as an active layer. The buffer layer 2 includes at least a silicon nitride film and protects the thin film transistor 3 from contamination by alkali metals such as Na and has a thickness such that it can shield the thin film transistor 3 from an electric field created by localized alkali metal icons (Na^+).

Yang '941 discloses that a thin film transistor which includes an oxide layer containing a trench; a semiconductor layer formed on the oxide layer, including the trench; a buffer layer formed on the semiconductor layer in the trench; a gate electrode aligned on the semiconductor layer on one side of the trench; and an impurity region formed in the semiconductor layer adjacent the gate electrode on one side of the trench, and an impurity region also formed in the semiconductor layer on the other side of the trench.

Shindo '640 discloses that a semiconductor device comprises a semiconductor layer including a source region, a drain region and a channel region provided on an insulating film. A gate insulating film separates the semiconductor layer from a gate electrode. A thickness of the channel region is smaller than a thickness of the source or drain region, and a level of an interface between

the channel region and the insulating film is different from a level of an interface of the source or drain region and the insulating film. All the surfaces of the channel region, source region and drain region which face the gate electrode are on the same level.

Hiroki *et al.* '717 discloses that a field effect type photo-detector comprises a semiconductor buffer layer arranged on a substrate. A semiconductor activation layer is arranged on that buffer layer, and a source electrode, a drain electrode and a gate electrode are arranged on the activation layer. A depletion layer for controlling a current flow between the source electrode and the drain electrode is created in the activation layer by applying a voltage to the gate electrode. When light irradiates the activation layer, the depletion layer changes. The buffer layer has a wider band gap than that of the activation layer and has an energy gap which serves as a barrier to carriers. The buffer layer has a sufficiently wide band gap to prevent the absorption of light having an equal wavelength to that of the light irradiated to the activation layer.

Wu '753 discloses that a process for manufacturing thin film transistors that have small source-drain areas, small gate-source parasitic capacitance C_{gs}, and low contact resistance, comprising producing the gate of the transistor on a glass substrate, depositing a gate insulating layer, a thick undoped amorphous silicon layer and a top passivation layer successively on the substrate. The top passivation layer and the thick undoped amorphous silicon layer are then etched until the insulating layer is exposed.

Ogura *et al.* '401 discloses that a thyristor has a laminated structure of a first emitter layer of n^+ conductivity type, a first base layer of p type, a second base layer of p^- type, a second emitter layer of n type, and a second emitter layer of p^+ type. The first base layer has a first exposed surface portion which is in lateral contact with the first emitter layer, and a second exposed surface portion which is in lateral contact with the second base layer. The second surface portion defines a layer portion of the second base layer which is positioned between the first base layer and the second emitter layer. An anode electrode is connected to said second emitter layer, whereas a cathode

electrode is connected to the second base layer and the first emitter layer. A first gate electrode is formed on the first surface portion of the first base layer. A second gate electrode is insulatively disposed above the second surface portion of the first base layer to form a MOSFET together with the first base layer and the second emitter layer. The layer portion of the second base layer serves as a channel region of the MOSFET.

Diem '930 discloses that process for producing by sloping etching a thin film transistor with a self-aligned gate with respect to its drain and source and transistor obtained by this process. The process consists of producing the transistor gate on a glass substrate, depositing an insulating layer on the substrate and gate, depositing a thick hydrogenated amorphous silicon layer on the insulating layer, depositing a positive photosensitive resin layer on the silicon layer, irradiating the resin layer through the substrate, the gate serving as an irradiation mask, developing the resin, chemically etching by successive, partial operations the silicon layer until the insulating layer is exposed, the remaining resin serving both as a mask and being etched following each etching operation of the silicon layer and producing the electrical contacts and source and drain electrodes of the transistor. Application to the production of active matrixes for liquid crystal flat screens.

Stoffel '661 describes a method for eliminating abnormalities in a polycrystalline silicon integrated circuit structure, such as a silicon gate field effect transistor structure. The layer of polysilicon is deposited on an insulator coating which may be the thickness of the gate dielectric. The polycrystalline silicon is delineated by lithographic techniques and a reactive ion etching process to form the desired conductor structure which would include gate electrodes for the field effect transistor structure. A thickness of the polycrystalline silicon of the order of hundreds of Angstroms is left upon the insulator coating where the masking layer has openings. This thin coating of polycrystalline silicon in the order of hundreds of Angstroms is then thermally oxidized together with the exposed sidewall of the polycrystalline silicon in the areas under the opaque parts of the masking layer to form silicon dioxide on the sidewall of the polycrystalline silicone structures. A directional reactive ion etching of the silicon dioxide removes all silicon dioxide formed by the

thermal oxidation step from the horizontal silicon substrate while leaving the silicon dioxide on the vertical sidewall regions. The method prevents the formation of a poor grade of silicon dioxide under the edges of the polycrystalline silicon conductor structure.

Dennard *et al.* '198 discloses that a method of fabricating a field effect transistor (FET) wherein a self-registered or misregistration tolerant electrical connection is provided between the gate electrode and a metallic interconnection line. The method involves a unique structure which includes a thick deposited oxide insulation layer and an etch stopping layer over doped silicon source and drain regions, over polysilicon gate electrode regions, and over field isolation regions. The etch stopping layer facilitates fabrication of a self-registering electrical connection between the gate electrode and a metallic interconnection line wherever desired. The thick deposited oxide layer provides reduced capacitive coupling between the insulated regions and the metallic interconnection line when compared to known self-registered gate contacting methods that employ only thermally grown oxide insulation. The method also includes the provision for controlling the removal of insulation over the gate electrode wherever desired without seriously degrading the insulation over other parts of the structure. The disclosed method further relates to fabricating an integrated circuit containing FETs having a self-registered electrical connection between the gate electrode and the metallic interconnection line, the gate electrode self-aligned with respect to the source and drain regions, and wherein FETs of the integrated circuit have: a channel region; a gate insulator; an electrically conductive gate electrode; source and drain regions; thick insulation over the source and drain and over the gate electrode except in the contact areas; field isolation or field shield regions between FETs of the integrated circuit; metallic-type high electrical conductivity interconnection line; and self-registering electrical connection between the gate and the interconnection line.

Currie *et al.* '812 discloses that a structure including a transistor and a trench structure, with the trench structure inducing only a portion of the strain in a channel region of the transistor.

Yamaguchi *et al.* '722 discloses that a power semiconductor device includes trenches

disposed in a first base layer of a first conductivity type at intervals to partition main and dummy cells, at a position remote from a collector layer of a second conductivity type. In the main cell, a second base layer of the second conductivity type, and an emitter layer of the first conductivity type are disposed. In the dummy cell, a buffer layer of the second conductivity type is disposed. A gate electrode is disposed, through a gate insulating film, in a trench adjacent to the main cell. A buffer resistor having an infinitely large resistance value is inserted between the buffer layer and emitter electrode. The dummy cell is provided with an inhibiting structure to reduce carriers of the second conductivity type to flow to and accumulate in the buffer layer from the collector layer.

Lochtefeld *et al.* '740 discloses that the benefits of strained semiconductors are combined with silicon-on-insulator approaches to substrate and device fabrication.

Yang '178 discloses a method for fabricating a flash memory having a T-shaped floating gate, comprising the steps of: forming a coupling oxide layer, a buffered layer, and a sacrificial layer in sequence on a semiconductor substrate; forming shallow trench isolation (STI); removing the portion of STI and said sacrificial layer so as to form a flat surface; forming a conductive layer; patterning said conductive layer so that a T-shaped floating gate is formed from the conductive layer and the buffered layer. The buffered layer and said conductive layer are made of a material selected from the group consisting of polysilicon, suicide and amorphous silicon wherein the buffered layer is formed to be 200 to 2500 .ANG. in thickness is and the conductive layer is formed to be 300 to 3000 .ANG. in thickness.

Hwang *et al.* '247 discloses that a method for fabricating an array substrate of a liquid crystal display device includes forming a gate line and a gate electrode connected to the gate line, forming a gate insulating layer, an amorphous silicon layer, a doped amorphous silicon layer and a metal layer on the gate line and the gate electrode, forming a data line, a source electrode, a drain electrode, an ohmic contact layer and an active layer by pattering the metal layer, the doped amorphous silicon layer and the amorphous silicon layer with a single photo-lithographic masking step, forming a

passvation layer covering the data line, and the source and drain electrodes, the passivation layer having a contact hole exposing a portion of the drain electrode, and forming a pixel electrode connected to the drain electrode through the contact hole.

Van der Zaag *et al.* '904 provides a method of manufacturing an electronic device including a vertical thin film transistor. A layer (8) of semiconductor material is provided over an insulated gate electrode (2). A negative resist (14) is used to define source and drain electrodes (26, 28) which extend over the insulating layer (8) up to the step formed therein adjacent an edge (16A) of the gate electrode (2).

Minami *et al.* JP'150 discloses that a gate oxide film 5, a gate electrode 6 and source-drain regions 1 and 2 are shaped into a region in a field oxide film 9 formed onto a p-type substrate 8 in succession. A side wall 7 is shaped on the side wall of the gate electrode 6, and polycrystalline silicon 12 is grown in an epitaxial manner at a low temperature onto the gate electrode 6 and single crystal silicon 3 and 4 onto the source-drain regions 1 and 2. Polycrystalline silicon on the gate electrode 6 is etched and the single crystal silicon films 3 and 4 are isolated, a passivation film 11 is formed, and contact holes 15 are shaped.

Anraku *et al.* JP'138 discloses that field oxide films 2, a first gate oxide film 3 and a first polycrystalline silicon layer 4 are forme din order on a single cyrstal silicon substrate 2. Then, an etching is performed on the first polycrystalline silicon layer 4 and the first gate oxide film 3, and by performing a vapor oxidation on the surface of the substrate 1 and the first polycrystalline silicon layer 4 at low temperatures, a polycrystalline silicon oxide film 6 and an oxide film 5 are formed. Then, when an etching is performed on the oxide film 5 and the polycrystalline silicon oxide film 6 to a degree that the substrate 1 is made to expose, the polycrystalline silicon oxide film 6 remains as the oxide film 6 is thicker than the oxide film 5. After this, when a thermal oxidation is performed at high temperatures, a second gate oxide film 7 is formed on the substrate 1, and at the same time, the polycrystalline silicon oxide film 6 becomes a thicker as the first polycrystalline

silicon layer 4I is oxidized through the polycrystalline silicon oxide film 6.

Kawarasaki *et al.* JP'464 discloses that a polycrystalline silicon film 8, to be a gate electrode, is deposited after a field oxide film 6 has been formed on a single crystal silicon film 5. The polycrystalline silicon 3 is subjected to an anisotropic plasma etching through a resist 10 as a mask using a photoengraving technique to form a gate electrode 8. Next, a source drain region 11 is formed by injecting impurity using the field oxide film 6 and the resist 10 as a mask. By these processes, even if depletion layers 12 extend from the source drain regions when a transistor is in operation, the layers 12 reach to a silicon oxide film 4 and are prevented from connecting each other by the oxide film 4. Therefore, the transistor is improved in breakdown strength and a semiconductor device, which is excellent in characteristic and has the advantage of being micronized, can be obtained.

Yamaguchi *et al.* JP'112 discloses taht the power semiconductor device includes a plurality of trenches (4) located in a first conduction type of a first base layer (1) spaced in a way of partitioning a main cell (MR) and dummy cells (DR) at positions apart from a second conduction type collector layer (3). A second conduction type of second base layer (7) and a first conduction type emitter layer (8) are placed in the main cell, and a second conduction type buffer layer (9) is placed in each dummy cell. A gate electrode (6) is located in each trench adjacent to the main cell via a gate insulation film (5). A buffer resistor with an infinite resistance value is inserted between the buffer layer and an emitter electrode. Each dummy cell is attached with a suppression structure (9a) for reducing the amount of first conduction carriers carried from a collector layer into the buffer layer and stored therein.

Kawasaki JP'337 discloses that On a substrate 100, a buffer layer 101, an activated layer 102 and a resist layer 103 are laminated in succession. Thereafter, a through hole 11 of T-shape in section, which reaches the activated layer 102, is formed, and metallic films 12, 13 are deposited extensively. Continually, the part of the metallic films 12, 13 for forming a gate electrode, which is

deposited on a resist film 103, is removed together with the resist film 103 by a lift-off method, and a gate electrode 14 of T-shape in section is formed. Then, after a thin film 15 is laminated extensively, using a reactive ion etching, the thin film 15 other than its part on the sidewall of the foot part of the gate electrode 14 is removed. Then, using the canopy top part of the gate electrode 14 as a mask, a metallic film 16 for forming an ohmic contact is deposited. Thereafter, a first metallic film 12 of the canopy top part of the gate electrode 14 is removed by a chemical dryetching. Further, a heat treatment is performed, and a source electrode 165 and a drain electrode 16D are formed.

Akiyama JP'432 discloses that an oxide film 102 is formed on a P-type silicon substrate 101 by the LOCOS method and a part of the surface of the silicon substrate on which an element is formed is oxidized to form an oxide film 103. Then, a polycrystalline silicon gate electrode 104 is patterned and phosphorus is injected by ion implantation to form low-density diffusion layers 105-1, 105-2. After a polycrystalline silicon film 106 and silicon oxide film 107 are deposited in sequence by the CVD method, the silicon oxide film is etched back by RIE and an insulated film 108 is formed on the side wall of the gate electrode 104. Next, the polycrystalline silicon film is etched and a silicon film 109 is formed. After that, arsenic is injected by ion implantation to form high-density diffusion layers 110-1, 110-2. Then, a layer-to-layer insulated film 111 and Al interconnections 112-1, 112-2 are formed. By this method, crystal defects are prevented from occurring and thus junction leakage current is reduced.

Yamamoto JP'634 discloses that an N-type drain region 2 is epitaxially grown on the surface of an N+-type silicon substrate 1, and a gate insulating oxide film 3 is formed thereon as thick as 40-150nm. A polycrystalline silicon layer is deposited thereon, which is etched using a photolithography technique to form a gate electrode 4. A P-type base region 5 is formed through implantation by the use of the gate electrode 4 as a mask. An oxide film 9 is formed on the surface of the gate electrode 4 taking advantage of the accelerated oxidation of polycrystalline silicon which also enables the activation and the forced diffusion of implanted ions. Then, the part of gate oxide film, which is not covered with the gate electrode 4 and the oxide film 9, is removed, and a nitride film 10 is formed.

The nitride film 9 is thermally oxidized to become thicker using the nitride film 10 as a mask. Next, the nitride film 10 is removed, and a source electrode 7 and a drain electrode 8 are formed of aluminum or the like.

Lee JP'860 discloses that a drift region and a source/drain ion implanted region are formed on the surface part of a substrate, a trench is made deeper than the drift region in the substrate and a channel 36 is formed along the bottom face part of the trench. A conductive films 38a for buffer is formed on the opposite sides of the trench while being separated and a gate electrode 42a is formed in between through an insulation film.

Kawamura JP'575 discloses that a silicon dioxide layer 6 is formed in a region, which is not masked with an ion implanting mask 41, in a polycrystalline silicon layer 3. After the mask 41 is removed, a silicon substrate is kept at the state the substrate is heated to about 500°C. Continuous wave argon laser of 8~10W is at a speed of 15 cm/sec. The polycrystalline silicon layer 3 at a region of a thickness of about 0.2μm at the upper part of the silicon dioxide layer 6 is converted into a single crystal silicon layer 7. The polycrystalline silicon layer 3 undergoes mesa etching, and an SOI substrate 31 comprising the single crystalline silicon layer 7 and the silicon dioxide layer 6 is formed. A gate insulating film 8 and a gate electrode 9 are formed. With the gate electrode 9 as a mask, n-type impurity ions are implanted, and a source 10 and a drain 11 are formed. Thus a MOS field effect transistor is formed.

Kwon KR'828 discloses that a groove portion is formed at a selected portion of a transparent substrate. The first metal pattern including a data line (42), a gate line (44) and a gate electrode (40) for a thin film transistor is formed in the groove portion. A gate insulating film and an active layer are orderly formed on the resultant structure. A source electrode (52) and a drain electrode (54) are formed on the active layer such that they are overlapped with the data line. A passivation layer is formed on the resultant structure and is then patterned to form the first contact hole (64) for exposing the drain electrode and the second contact hole (62,66) for exposing the data line and the source

electrode at the same time. A metal film is deposited on the resultant structure and is then patterned to form a pixel electrodes (68) electrically connected to the drain electrode and a link electrode (70) commonly connected to the data line and the source electrode.

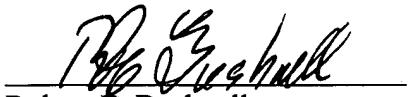
Eom KR'124 discloses that after forming a gate oxide layer(2A) on a silicon substrate (1), a polysilicon layer(3) and a tungsten silicide layer (4) are sequentially formed on the gate oxide layer. A gate electrode is formed by sequentially patterning the tungsten silicide layer (4), the polysilicon layer (3) and the gate oxide layer (2A). The gate electrode is then annealed at the temperature of 750-850 °C in N2O gas atmosphere, wherein fluorine(F) is inactivated.

Kawachi *et al.* JP'135 discloses that elements are separated by using low temperature plasma oxidation to form such a structure that a gate insulating film is not in contact with the side face of the semiconductor pattern of a TFT so as to prevent a parasitic channel on the side face of the semiconductor pattern. By this method, since the side face of the semiconductor pattern is not in contact with the gate insulating film, no parasitic channel is formed on the side face. Moreover, no step is formed in the end of the semiconductor pattern so that a dense and high-quality insulating film which is inferior in the step coverage can be used, and this improves the reliability.

The citation of the foregoing references is not intended to constitute an assertion that other or more relevant art does not exist. Accordingly, the Examiner is requested to make a wide-ranging and thorough search of the relevant art.

No fee is incurred by this Statement.

Respectfully submitted,



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	APPLICANT HOON KIM	
	FILING DATE 12 March 2004	GROUP 2826

U.S. PATENT DOCUMENTS

EXAMINER	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,777,747	08/04	Yedinak *et al.*	257	339	
	6,534,788	03/03	Yeo *et al.*	257	072	
	6,528,855	03/03	Ye *et al.*	257	401	
	6,509,234	01/03	Krivokapic	438	270	
	6,396,079	05/02	Hayashi *et al.*	257	066	
	6,033,941	03/00	Yang	438	163	
	5,510,640	04/96	Shindo	257	347	
	5,196,717	03/93	Hiroki *et al.*	257	021	
	5,173,753	12/92	Wu	999	023.700	
	5,144,401	09/92	Ogura *et al.*	999	038	
	4,715,930	12/87	Diem	999	101	
	4,287,661	09/81	Stoffel	438	303	
	4,035,198	07/77	Dennard *et al.*	438	297	
	2004-0173812	09/04	Currie *et al.*	257	103	
	2004-0084722	05/04	Yamaguchi *et al.*	257	330	
	2004-0005740	01/04	Lochtefeld *et al.*	438	149	
	2003-0122178	07/03	Yang	257	314	
	2002-0054247	05/02	Hwang *et al.*	349	043	
	6,746,904	06/04	Van der Zaag *et al.*	438	149	

EXAMINER: *DATE CONSIDERED:*

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT PTO-1449 (PAGE 2 OF 2)	SERIAL NUMBER 10/798,574	DOCKET NO. P57012
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FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	JP 63-093150	04/88	JAPAN			Abstract	
	JP 61-078138	04/86	JAPAN			Abstract	
	JP 02-031464	02/90	JAPAN			Abstract	
	JP 2004-153112	05/04	JAPAN			Abstract	
	JP 04-096337	03/92	JAPAN			Abstract	
	JP 04-101432	04/92	JAPAN			Abstract	
	JP 02-281634	11/90	JAPAN			Abstract	
	JP 2002-329860	11/02	JAPAN			Abstract	
	JP 01-128575	05/89	JAPAN			Abstract	
	KR 010082828	08/01	REPUBLIC OF KOREA			Abstract	
	KR 100332124	03/02	REPUBLIC OF KOREA			Abstract	
	JP 2001-125135	05/01	JAPAN			Abstract	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

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